Beam Test LBNL Phase-2 Telescope

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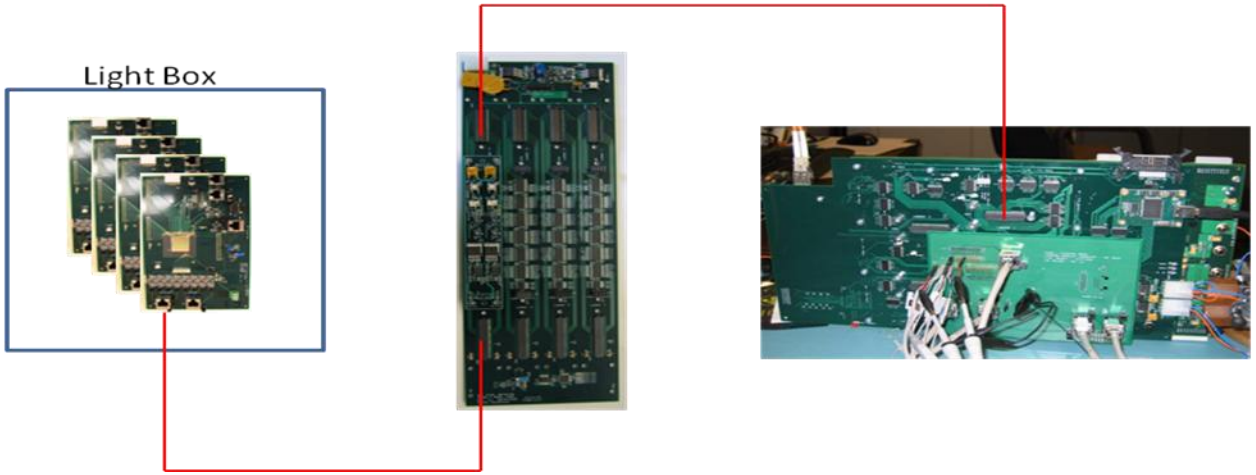
Schematic Setup / Components



- 4-sensor telescope (Phase-2) in a light-tight box
- Scintillator trigger
- LU-protected power and buffering (Mass Termination Board, MTB)
- Motherboard / Xilinx Virtex-5 Eval-board combo with DDL-SIU
- Bench Power supply
- RDO PC with DDL-RORC
- Oscilloscope

Purpose and General Idea

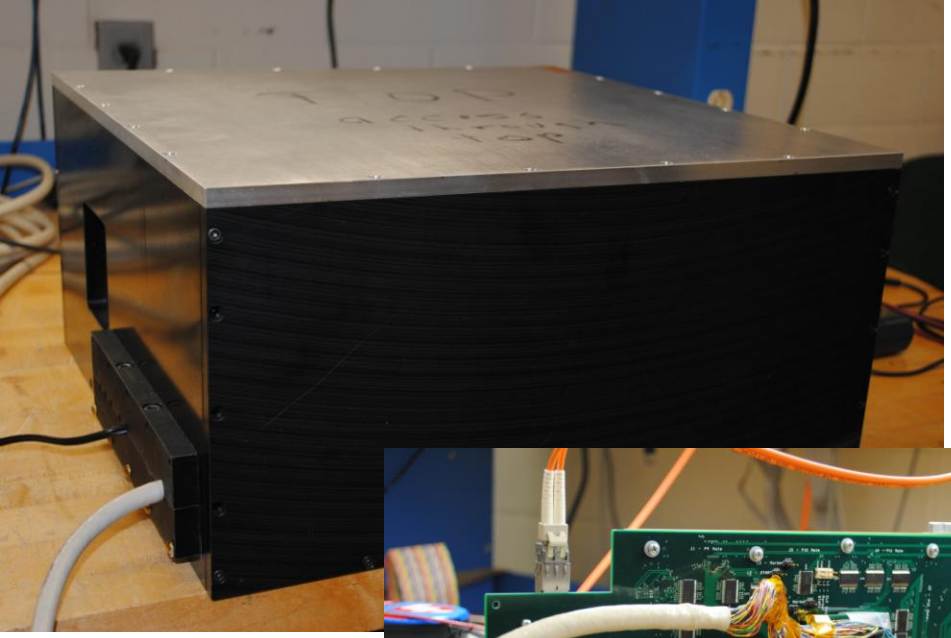
- Measure sensor efficiency & resolution as a function of
  - Threshold
  - Bias settings
  - Voltage
  - Other?
- Use MIPS at a beam test facility to penetrate 4 sensors arranged in a telescope configuration
- Resulting tracks should be analyzed online to guide settings
- Depending on beam structure, triggering through scintillators placed before and after the telescope might be necessary for the FPGA based readout
- If there is a flattop type spill, maybe continuous readout?
- Possible analog readout for 1 (front) of the sensors?

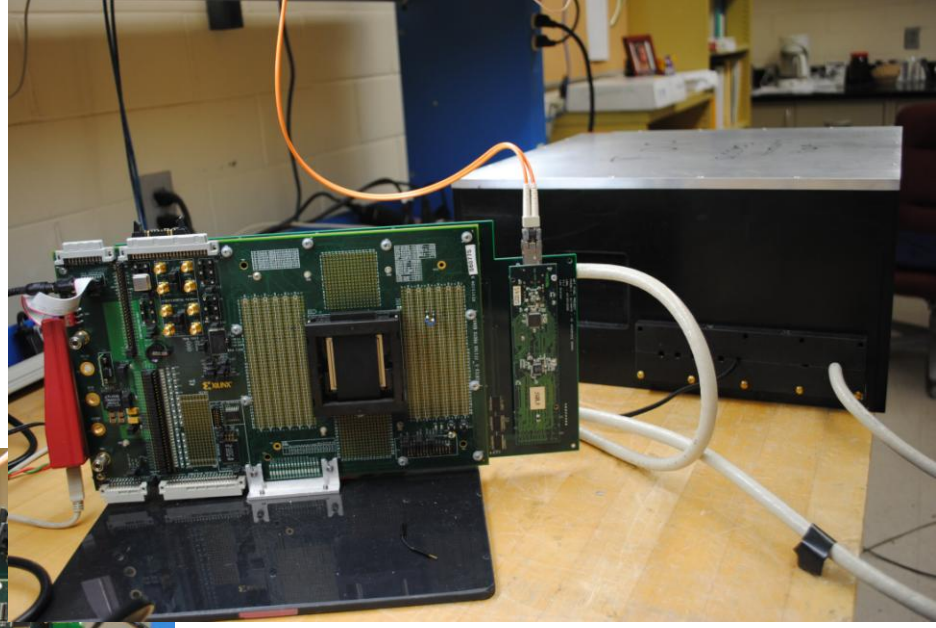
Possible Test Beam Locations

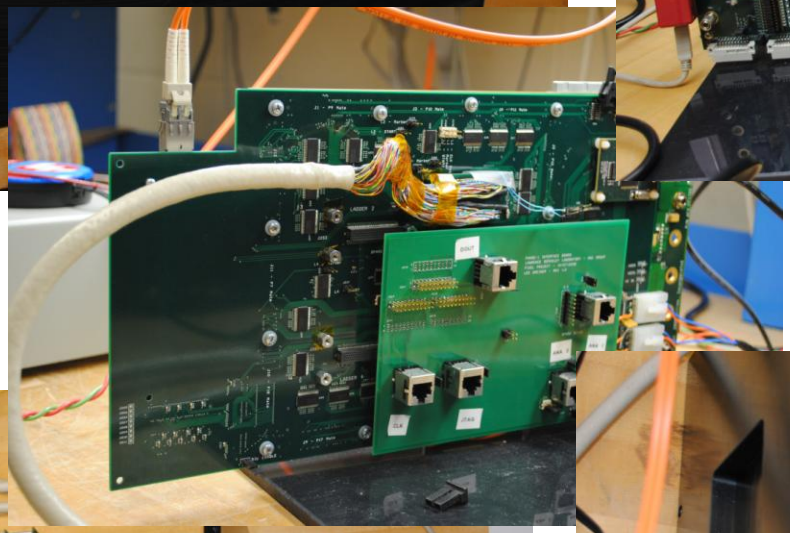
- CERN: 2 test beam areas: East Area, West Area
  - 1 – 15 GeV mixed, 24GeV protons
  - available May – mid November
- DESY: 3 test beam lines
  - 1 – 6 GeV electrons
  - available until July 10 & mid August – mid December
- FNAL: Meson Detector Building West
  - large administrative overhead, need full proposal
  - 120 GeV protons, 2 – 66 GeV pions, 0.7 – 32 GeV electrons
  - Schedule?
- SLAC: new test beam ESTB
  - 4 – 14 GeV electrons
  - mid July – Christmas (?), downtime Aug/Sep (?)

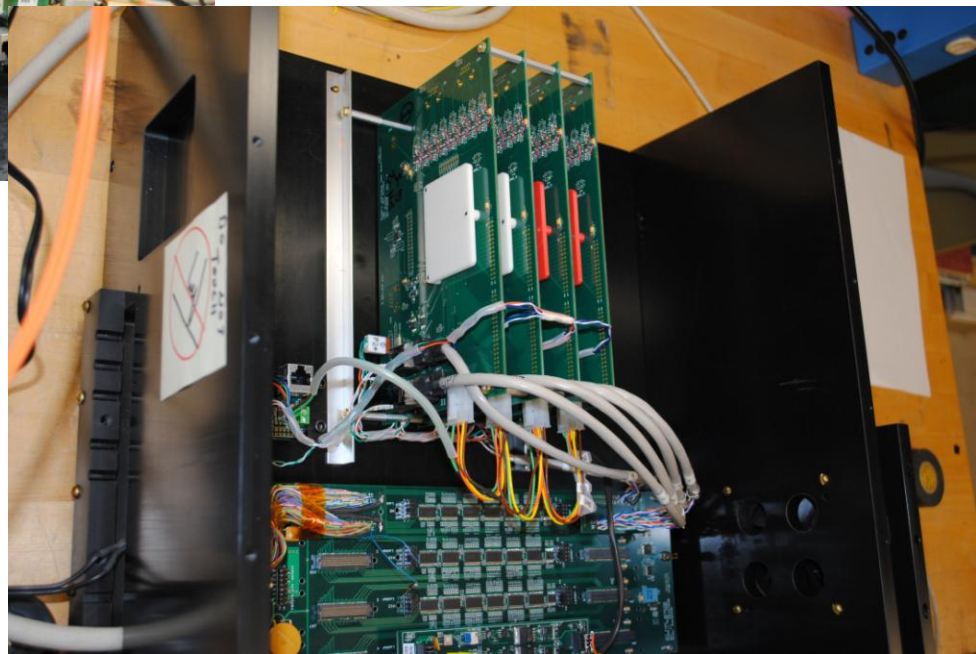
Hardware Status & Plans

- Light-tight box built with fan and mounts for sensor test boards & MTB (see pictures).
- Scintillators still need to be put together and mounted in the box. Electronics for these should be available at UT
  - Alternatively, just use a beam spill signal, since frame covers a lot of beam particles
- Individual sensor boards are of the same architecture as used for Ultimate testing, so once Ultimate is ready, it should be a drop-in replacement
- The cabling of the 4-sensor setup has been tested with the Virtex-5 board, and is now functional, after some initial issues with the JTAG lines between the boards.
- Possibly build a spare twisted pair cable bundle between box and RDO; current cable somewhat fragile. Possibly bring existing cable from LBL









Firmware Status & Plans

- Firmware written by X. Sun for 10-sensor ladder test has been modified to accommodate 4-sensor readout in individual frames
- Control Interface via DDL fiber link or QuickUSB I/F board. DDL works only under Linux, QuickUSB currently only works (reliably) under Windows
- Data Acquisition over either USB (Windows) or DDL (Linux)
- SRAM (on mother board) based FIFO used to buffer full frames
- JTAG state machine controls sensors in response to commands
- ADC can be used to read analog data
- LVDS signal path skews are taken care of inside FPGA via adjustable I/O-delays for each signal, uploaded via command interface
- Readout sends 2 full frames worth of data, up to an adjustable number of data words
- Currently, internal firmware generated trigger is used for readout, need to write firmware to respond to external triggers

Software Status & Plans

- Linux programs exist for the following tasks to interface with FPGA:
  - Sending commands (including jtag) over DDL to FPGA
  - Receiving data over DDL from FPGA
  - Assembling commands in the proper format
  - I/O-delay data analysis and parameter determination
- Several scripts exist to combine the above programs for specific tasks
- LabView GUI to set control register parameters and convert them to appropriate jtag command sequences (currently only in Windows)
- Root analysis of sensor data (used for threshold scans and simple analysis)
- Still Needed:
  - Data acquisition programs
  - Analysis programs for telescope (Root, Python, Qt)
  - “Online” (live) data analysis to check data quality
- Analysis tasks needed:
  - Tracking
  - Correlations
  - ???

Schedule

- As soon as possible…
- Just got hardware to work reliably
- Need additional time for firmware extensions and additional software development
- Depends on chosen facility availability, of course
- About 1 shift setup, ~ 3 (?) shifts data taking